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| 10/743,401 | 12/22/2003 | Timothy J. Dupuis | SIL.P0068 | 7172 |

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| EXAMINER |
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NGUYEN, DUC M

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| ART UNIT | PAPER NUMBER |
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2618

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08/27/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/743,401

Applicant(s)

DUPUIS, TIMOTHY J.

Examiner

Duc M. Nguyen

Art Unit

2618

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 June 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-19,21-40 and 43-45 is/are pending in the application.
- 4a) Of the above claim(s) 7-13,15-19,22-29 and 31-40 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 3-6, 14, 18, 21, 30, 43-45 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date: _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This action is in response to applicant's response filed on 10/12/04. Claims 1, 3-6, 14, 18, 21, 30, 43-45 are now pending in the present application. **This action is made final.**

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims **1, 30, 45** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Blake et al (US 6,847,904)** in view of **Nalbantis (US 2004/0148553)**.

Regarding claim **1**, **Blake** discloses an RF amplifier formed using an integrated circuit (see Fig. 1 and Abstract), comprising

- A amplifier (see Fig. 1) and
- A serial interface formed using the integrated circuit for sending and receiving signal (see Fig. 1 and col. 5, line 25 – col. 6, line 7).

Although **Blake** does not specifically disclose the PGA amplifier is the power amplifier, one skilled in the art would recognize that an power amplifier would work equally well with Blake's teaching regarding serial interface formed using the integrated circuit. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to apply Blake's teaching to a power amplifier, for utilizing

Art Unit: 2618

advantages of the serial interface such minimizing pin count of the IC package (see col. 5, lines 55-60). Therefore, the claimed limitation regarding the power amplifier is made obvious by Blake.

Further, since Blake teaches a chip select CS pin for controlling functions either in the "shifting data" mode or in the "latching" data mode (see col. 5, line 55 – col. 6, lines 7), it is clear that the chip select CS pin would act as the mode control pin SEN taught by **Nalbantis** (see [0030] regarding mode control pin SEN and "shifting data" or "latching" data). Therefore, the claimed limitation regarding the mode control pin is made obvious by Blake and Nalbantis, wherein the "shifting data" mode would read on the first mode/function, and the "latching" data mode would read on the second mode/function.

Regarding claim **30**, the claim is rejected the same reason as set forth in claim 14 above. In addition, since using a baseband controller to adjust the gain of the power amplifier is well known in the art, it would have been obvious to one skilled in the art at the time the invention was made to further modify Blake for providing a baseband controller as claimed, in order to control the output gain of the power amplifier.

Regarding claim **45**, the claim is rejected the same reason as set forth in claim 30 above. In addition, since **Blake** teaches the serial interface is used control the function of the amplifier such as gains, bandwidth, power consumption, input offset correction, frequency response, etc, (see col. 2, lines 23-42 and Fig. 1), it is clear that Blake as modified would obviously teach a band control signal utilizing the serial bus as claimed,

Art Unit: 2618

in order to select a band based on the band control signal (see Fig. 1 regarding MUX 104).

3. Claims **3-4, 14, 18, 20, 43-44** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Blake** in view of **Nalbantis** and further in view of **Tomasz** (US **6,400416**).

Regarding claim **3**, the claim is rejected the same reason as set forth in claim 2 above. In addition, although **Blake** teaches the serial interface is used control the function of the amplifier such as gains, bandwidth, power consumption, input offset correction, frequency response, etc, (see col. 2, lines 23-42), **Blake** is silent with a second interface pin having a first function/mode and a second/function mode. However, **Tomasz** teaches a method for adjusting the gain of an amplifier, wherein **Tomasz** suggests that the gain may be adjusted either by a dedicated external pin on the IC circuit or via a serial bus (see col. 6, lines 32-42). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to further incorporate **Tomasz's** teaching to **Blake's** as well, for further providing an external pin for controlling the gain of the amplifier as well, thereby providing a second interface pin with a mode control pin as claimed, in order to achieve various control functions for the amplifier either via the external pin or via the serial bus pins.

Regarding claim **4**, the claim is rejected the same reason as set forth in claim 3 above. In addition, **Blake**, in view of **Tomasz**, as modified would teach the first mode is a serial interface mode (serial input pins) and the second mode is a pin control mode

(external pin), in order to controlling the gain of the amplifier via the external pin or via the serial bus pins.

Regarding claim **14**, the claim is rejected the same reason as set forth in claim 4 above. In addition, since one skilled in the art would recognize that the amplifier circuit as disclosed by Blake would applicable to a wireless transceiver and would work equally well, it would have been obvious to one skilled in the art at the time the invention was made to further modify Blake for providing a transceiver coupled a serial bus as claimed, for utilizing advantages of the serial interface in Blake such as minimizing pin count of the IC package (see col. 5, lines 55-60) for controlling the transceiver.

Regarding claim **18**, the claim is rejected the same reason as set forth in claim 14 above. In addition, since **Blake** teaches the serial interface is used control the function of the amplifier such as gains, bandwidth, power consumption, input offset correction, frequency response, etc, (see col. 2, lines 23-42 and Fig. 1), it is clear that Blake as modified would obviously teach a band control signal utilizing the serial bus as claimed, in order to select a band based on the band control signal (see Fig. 1 regarding MUX 104).

Regarding claim **20**, the claim is rejected the same reason as set forth in claim 4 above.

Regarding claim **43**, the claim is rejected the same reason as set forth in claim 3. above.

Regarding claim **44**, the claim is rejected the same reason as set forth in claim 4 above.

4. Claims **5-6** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Blake** in view of **Nalbantis** and further in view of **Richard et al** (US **6,894, 266**).

Regarding claim **5**, the claim is rejected the same reason as set forth in claim 1 above. In addition, since the IC package in Blake would require a power supply to operate, it would have been obvious to one skilled in the art at the time the invention was made to provide the internal voltage source via a control pin as disclosed by **Richard** (see col. 5, lines 32-37 and col. 6, lines 20-35), in order to provide the supply voltage for registers of the IC package while minimizing the number of pins for the IC packages.

Regarding claim **6**, the claim is rejected the same reason as set forth in claim 5 above. In addition, **Richard** discloses the pin is used to supply power in the serial-in fashion only (see col. 5, lines 37-38).

5. Claims **5-6** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Blake** in view of **Nalbantis** and further in view of **Collins et al** (US **5,724,009**).

Regarding claim **5**, the claim is rejected the same reason as set forth in claim 1 above. In addition, since the IC package in Blake would require a power supply to operate, it would have been obvious to one skilled in the art at the time the invention was made to provide the internal voltage source via a control pin as disclosed by **Collins** (see col. 2, line 58 – col. 3, line 7), in order to provide the supply voltage for

Art Unit: 2618

digital circuitry (registers) of the IC package while minimizing the number of pins for the IC packages.

Regarding claim **6**, the claim is rejected the same reason as set forth in claim **5** above. In addition, since the supply voltage is used for operating the digital circuitry, it is clear that it is used as internal voltage source only for serial data input (shifting data mode).

6. Claim **21** is rejected under 35 U.S.C. 103(a) as being unpatentable by **Blake** in view of **Nalbantis** and **Tomasz**, and further in view of **Collins et al** (US **5,724,009**).

Regarding claim **21**, the claim is rejected the same reason as set forth in claim **20** above. In addition, since the IC package in **Blake** would require a power supply to operate, it would have been obvious to one skilled in the art at the time the invention was made to provide the internal voltage source via a control pin as disclosed by **Collins** (see col. 2, line 58 – col. 3, line 7), in order to provide the supply voltage for digital circuitry (registers) of the IC package while minimizing the number of pins for the IC packages.

Response to Arguments

7. Applicant's arguments filed 6/29/07 have been fully considered but they are not persuasive.

As to claims **1**, **30**, Applicant contends that

Blake discloses a programmable gain amplifier. **Blake** shows an op-amp **102** formed on an integrated circuit **100**. The integrated circuit **100** includes a serial peripheral interface **106**.

Art Unit: 2618

Blake does not teach or suggest a mode selection pin that is used to select first or second mode of operation. In addition, Blake does not teach or suggest an interface pin that has different functions in first and second modes of operation. An advantage of one example of a power amplifier of the present invention is that it can operate in different modes, where one or more pins have different functions, depending on the mode selected. For example, FIG. 2 of the present application illustrates various interface pins, and shows functions of the pins for different modes. For example, one pin is shown as being used as a serial data input (SDI) pin in one mode, and as a voltage reference (VDD) pin in another mode. Of course, these are just examples, and the claims are not limited to the examples shown in the figures.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., one pin is shown as being used as a serial data input (SDI) pin in one mode, and as a voltage reference (VDD) pin in another mode) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Here, since **Blake** in view of **Nalbantis** would teach a mode control pin for controlling functions either in the "shifting data" mode or in the "latching" data mode (see **Blake**, col. 5, line 55 – col. 6, lines 7 and **Nalbantis**, [0030] regarding mode control pin SEN and "shifting data" or "latching" data), the "shifting data" mode would read on the claimed first mode/function, and the "latching" data mode would read on the claimed second mode/function as recited in claims 1, 30.

As to claim 14, Applicant contends that

Amended claim 14 recites a wireless communication device comprising "a controller circuit adapted to control the operation of the communication device," "a transceiver," "an RF power amplifier having a mode control pin and a first interface pin, wherein the state of the mode control pin determines whether the RF power amplifier operates using a serial interface mode or a pin control mode, and wherein the first interface pin has a first function in the serial interface mode and a second function in the pin control mode," and "a serial bus coupled to the controller, transceiver, and RF power amplifier."

Art Unit: 2618

For at least the reasons set forth above with respect to amended claim 1, applicant asserts that amended claim 14 is allowable over the prior art. Since dependent claims 18 and 21 depend from amended claim 14, it is also believed that these claims are allowable over the prior art.

In response, the examiner asserts that although **Blake** teaches the serial interface is used control the function of the amplifier such as gains, bandwidth, power consumption, input offset correction, frequency response, etc, (see col. 2, lines 23-42), and that **Blake** is silent with a second interface pin having a first function/mode and a second/function mode, it is noted that **Tomasz** teaches a method for adjusting the gain of an amplifier, wherein **Tomasz** suggests that the gain may be adjusted either by a dedicated external pin on the IC circuit or via a serial bus (see col. 6, lines 32-42). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to further incorporate **Tomasz's** teaching to **Blake's** as well, for further providing an external pin for controlling the gain of the amplifier as well, thereby providing a second interface pin with a mode control pin as claimed, in order to achieve various control functions for the amplifier either via the external pin or via the serial bus pins. Therefore, **Blake**, in view of **Tomasz**, as modified would teach the first mode is a serial interface mode (serial input pins) and the second mode is a pin control mode (external pin), in order to controlling the gain of the amplifier via the external pin or via the serial bus pins.

For foregoing reasons, the examiner believes that the pending claims (1, 3-6, 14, 18, 21, 30, 43-45) are not allowable over the cited prior art.

Conclusion

Art Unit: 2618

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. **Any response to this final action should be mailed to:**

Box A.F.

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(571) 273-8300 (for **formal** communications intended for entry)

(571)-273-7893 (for informal or **draft** communications).

Hand-delivered responses should be brought to Customer Service Window, Randolph Building, 401 Dulany Street, Alexandria, VA 22314.

Any inquiry concerning this communication or communications from the examiner should be directed to Duc M. Nguyen whose telephone number is (571) 272-7893, Monday-Thursday (9:00 AM - 5:00 PM).

Application/Control Number: 10/743,401

Page 11

Art Unit: 2618

Or to Matthew Anderson (Supervisor) whose telephone number is (571) 272-4177.

Duc M. Nguyen, P.E.

Aug 23, 2007

A handwritten signature in black ink, appearing to read 'Duc M. Nguyen', with a long horizontal flourish extending to the right.